Very High Pin Count Flip Chip Assembly Using Conductive Polymer Adhesives

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Abstract

High pin count flip chip assembly is becoming increasingly necessary for many sensor applications. Electroplated solder bumping technology provides one means for achieving fine-pitched flip chip assembly, but is not an allowable option for many temperature sensitive and microelectromechanical (MEMS) applications. Indium bump bonding, also known as "hybridization", is another common technique, but requires high pressure for cold-welding the bumps together. An alternative polymer adhesive approach is described in this article, which combines Au-wire stud bumped devices with stencil printed conductive epoxy that can be printed at pitches below 200µm and cured at temperatures as low as 80°C. Flip chip test chips with pin counts as high as 8000 I/O have recently been assembled and are discussed and illustrated.

Key Words: Adhesive Flip Chip, Indium Bump Bonding, Au-Stud Bump, Hybridization, CdZnTe Detector, CZT, IR Focal Plane Array

1. Introduction

High-density flip chip assembly combined with low-temperature processing is emerging as a critical path for the successful development of many sensor and imaging devices. A variety of compound semiconductor materials, manufactured from II-VI and III-V group materials, are being developed for hard x-ray/gamma-ray and IR imaging devices (e.g., CdZnTe, HgCdTe and HgI_2 detectors). Applications range from near-space, in the form of medical and airport security devices, to deep-space astronomical applications. Many of these sensors employ fine-pitched, pixel array patterns requiring very high pin counts - in excess of 1000 interconnections - and are limited to processing temperatures below 100°C. [Although an exact definition for "very" high pin count is necessarily subjective, for the purpose of this paper I am including any flip chip device with 1000 or more bump connections.]

2. Range of Flip Chip Technologies Available

At present there are at least a dozen different methods for bumping and bonding flip chip devices to the surface of a substrate. The choice of flip chip bumping processes include, electro- and electroless plated gold bumps, gold wirebonded (stud) bumps, stencil printed solder or conductive epoxy bumps, and evaporated, sputtered or electroplated solder bumps deposited on either an individual chip or whole wafer. After the device is placed onto the substrate, flip chip bonding may be accomplished by reflowing the solder bumps, or by curing isotropic or anisotropic conductive adhesives, or by fusion-bonding with pressure alone. Another option is snap-curing non-conductive adhesives, pre-applied as an underfill, using a thermocompression bonder. Of course, there are many variations of materials and processes for each of these flip chip techniques that the reader may be aware of. Unfortunately, almost all of these examples involve high temperatures (and/or high normal forces during placement) and, therefore, may not be practical or technically feasible for assembling temperature sensitive or fragile detectors and imaging devices.

Other devices, presently in development and expected to be restricted to low temperature assembly processing, include DNA analyzers, bio-medical MEMS, organic and polymer LED displays, and polymer memory chips. To my knowledge, there are only two flip chip assembly techniques, presently in widespread usage that would qualify as practical low-temperature processes; these are indium bump bonding and adhesive bonding using conductive (isotropic) epoxy. Although other direct chip attach (DCA) technologies, such as micro-springs or micro-piercing structures, have been reported in the literature and may eventually become practical methods for low-temp flip chip assembly, they

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appear to still be in the realm of experimental development and therefore beyond the scope of this paper.

3. Indium Bump (*Hybridization*) Bonding

Since image resolution is a function of the number of pixels, there is a continuing need to push for higher interconnect (I/O) density by reducing the pitch between pixel elements. Currently, indium bump bonding (or "*hybridization*" as it is commonly called) is the prevailing ultra fine-pitch, flip chip methodology. Several government and private research labs are capable of performing this process at pitches as small as 50µm; however the current '*state of the art*' is closer to 18-20µm pitch.

The process begins with vacuum deposition of an Under Bump Metallization (UBM) layer over the metal pads of both surfaces to be joined to prevent diffusion of the indium. Pure indium metal is then e-beam (vapor) deposited onto the UBM metal using either a shadow mask or photoresist lift-off technique to define the bump geometries. The indium bumps are typically only 15-20µm in diameter and 7-10µm thick at these pitches, resulting in the surfaces being separated by only 8-15µm after assembly. Obviously, flatness of the surfaces and uniformity of the indium bump heights are critical to the success of this process.

Unlike solder bump deposition, the indium bumps are not reflowed prior to assembly, leaving their morphology somewhat jagged in appearance (see Figure 1). This "jagged" topology presumably aids in the joining process by enabling the top surfaces of the bumps to be more deformable and likely to rub through non-conductive surface oxides during the cold or low-temperature fusion process. The bump-to-bump fusion process requires high normal forces (1-2g/bump) during assembly. Here then is the primary problem with indium bump bonding -- as the surface area increases, along with commensurate number of fine-pitched bumps, the pressure required to achieve reliable interconnect also increases, creating the potential for damage. Adding heat to the process may render the indium bumps more malleable, but can also introduce residual strain and the potential for shear-fractures developing in the joined bumps after the parts cool to room temperature. Since these image sensors cannot typically operate properly with an epoxy underfill present, either the materials being joined must be closely matched for coefficient of thermal expansion (CTE), and/or the joining process must be performed as close to room temperature as possible, especially, since many of these devices are intended to be operated at sub-zero temperatures. Needless to say, indium bump bonding is perhaps the most expensive flip chip process current and therefore is chosen for only the most demanding applications.

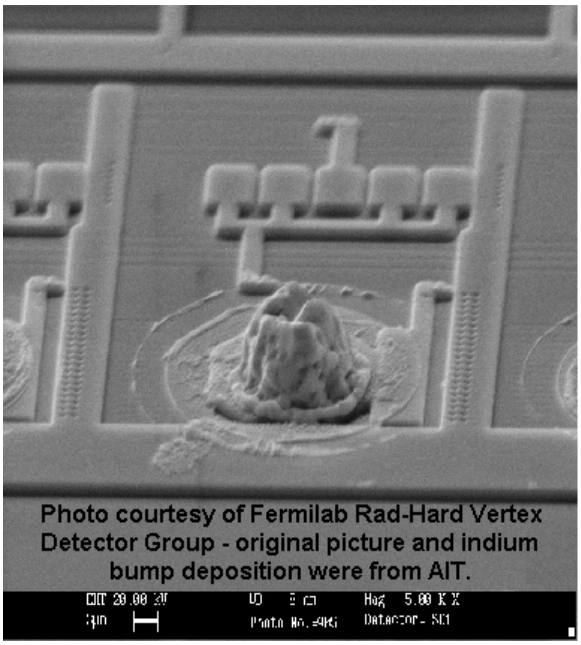

Figure 1: SEM photo of a vacuum-deposited indium bump (~15-20µm diameter).

Electroplated solder bumps compare favorably with evaporated indium bumps and can be deposited at pitches as small as 20µm. However, the typical solder alloys that can be easily electroplated require reflow temperatures exceeding 212°C [1]. And, with the push to eliminate all lead from solder, the processing temperatures have now risen as high as 265°C.

Anisotropic adhesives are noted for their ability to achieve fine interconnect of LCD driver chips to flex circuits and flex-to-ITO (Indium-Tin-Oxide) traces on glass substrates, but require both high bonding temperature and pressure. That leaves isotropic conductive adhesive as the only remaining flip chip process that can meet the requirement for low temperature processing.

4. Au-Stud Bump Bonding

Wirebonding has long exceeded its predicted obsolescence. One needs only to see how this technology has been creatively adapted for 3D packaging of stacked chips or fashioned into micro-spring contacts to appreciate its versatility. Of particular importance for flip chip assembly are the dedicated, high-speed, gold-stud bump bonders that are now available. These machines are capable of applying between 10-15 stud bumps per second with placement accuracy of +/- 2-5µm. Recent reports mention continuing improvements in reducing wirebond ball diameter (and hence pitch between

adjacent bumps) and process compatibility with low-K dielectrics.

Au-stud bumps are simply modified thermosonic wirebond connections in which the wire has been purposely severed from the ball-bond, leaving only the Au-ball (*stud-bump*) attached to the chip's bond-pad. A major advantage of this technique is that the thermosonic ball-bonding process scrubs through the aluminum oxides present on typical IC pads, eliminating any need to pre-apply any UBM layer. Reliable, low-impedance, metal-to-metal interconnects are a distinct characteristic of this technology and a principle reason why it has remained in favor for so long. Solder or conductive epoxies, conversely, require a compatible metal surface for reliable connections. Silver-filled conductive epoxies, for example, perform best in contact with noble metal-finishes such as Au, Pt or Pd, but will not provide a reliable connection in direct contact with untreated aluminum. Fortunately, the industry trend towards all copper interconnect at the IC level, instead of aluminum, may make UBM a thing of the past, since the Cu-pads are expected be finished with a thin Ni-Au layer.

Gold-stud bump bonding is ideal when only a few devices need to be bumped, but is not a particularly efficient process when attempting to bump an entire wafer. Depending on the number of contacts per device, a single wafer may tie up a bonder for 8-12 hours. Nevertheless, the process is extremely clean and relatively economical, since no chemicals are involved and so little material is consumed in forming the individual ball bumps.

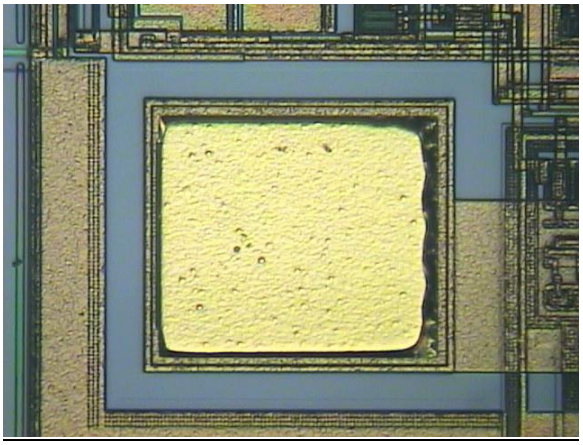

Figure 2: Close-up photo of an electroless (Ni-Au) plated pad.

The most economical bumping process presently available, for handling whole wafers, is electroless-plated nickel-gold (Ni-Au) bumps. This process typically deposits between 5-25µm of Ni over the aluminum pads through a zincate process after etching away the surface oxides. A thin Au coating is then plated over the Ni to prevent oxidation of the Ni-bumps (see Figure 2). This immersion plating process has proven to be fairly benign to most CMOS devices and rarely requires any masking step. The process is commonly employed for bumping RFID and Smartcard chips for flip chip assembly onto flexible inlets - an application that is extremely cost sensitive.

5. Flip Chip Assembly with Conductive Adhesives

Silver-filled conductive epoxies have been around for over thirty years, but have been substantially bypassed in the US for most flip chip applications in deference to solder. The same is not true in Japan and Europe, where these materials have received far more interest and study and are presently being used in high volume assembly of inexpensive mobile products. One might argue that most manufacturing and packaging engineers here in the US are understandably reluctant to depart from "tried and true" solder-alloys with which they are familiar; but the market-driven need to find non-lead alternatives is creating a renewed interest in these materials, especially considering that future integrated chips may be based on polymer substrates instead of silicon.

In Japan, flip chip assembly with conductive epoxies is almost exclusively used in combination with Au-stud bumped chips. The tips of the Au-stud bumps are first dipped into a thin layer of the epoxy that has been spread across the surface of a rotating platter using an adjustable doctoring blade, and then transferred to the substrate pads when the chip is aligned and placed onto the substrate. This technique, commonly referred to as "*dip-transfer*", is becoming increasing more available as an option on many flip chip placement machines, pointing to its successful implementation in Asian assembly houses. The process is particularly well suited when it becomes necessary to assemble flip chip devices onto circuit boards already populated with soldered components – so called "mixed technology". Regulating the amount of epoxy material transferred onto the Au-stud bumps is critical for ensuring high assembly yields, since electrical shorts may develop between adjacent bumps, either from bridging during the dip process itself, or from epoxy spreading during chip placement.

6. Stencil Printed Polymer Bumping

An alternative assembly process involves stencil printing the conductive ink directly onto the device or substrate, and then aligning and placing the Au-stud bumps disposed on the other piece into the epoxy bumps while they are still wet. In this manner, the epoxy is less likely to short between adjacent

bumps, since the amount of epoxy can be more carefully regulated. In addition, a more robust contact between the epoxy and the substrate pad is established by virtue of the bump contour. In profile, stencil printed polymer bumps resemble a rounded volcano, as shown in Figure 3.

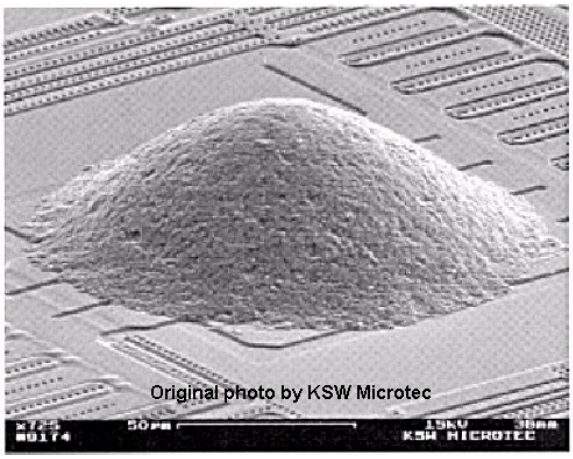

Figure 3: Stencil printed, conductive epoxy bump (~150µm diameter).

As with indium bump bonding, the uniformity of the Au-stud bump and stencil printed bump height are also critical when working with conductive (isotropic) epoxies for flip chip assembly. If the Au-stud bumps are not of equal height above the chip's surfaces, they may not "pick-up" a sufficient amount of epoxy when using the *dip-transfer* method, or penetrate far enough into the pre-applied bumps of the substrate to ensure reliable electrical contact. One could argue, however, that the stencil printing method is more tolerant of stud bump height variation, since the chip's Au-stud bumps typically penetrate the full thickness of the printed epoxy bumps until they touch the underlying pads.

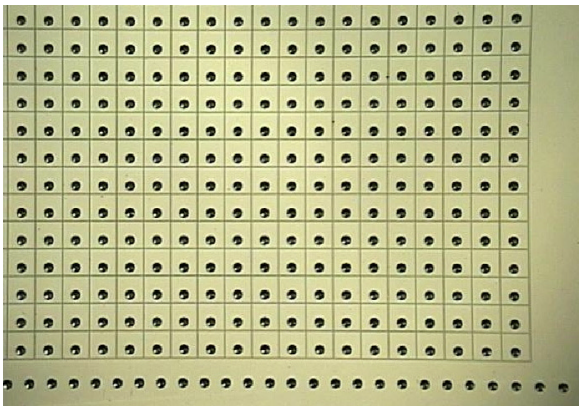

Figure 4: A portion of a 24X44 CdZnTe pixel-array with conductive epoxy bumps spaced 498µm apart. The bumps are purposely offset from the center-point of each pixel.

7. CdZnTe Detector Assembly

Figure 4 illustrates an example of a CdZnTe (or CZT) detector populated with an array of over 1056 polymer bumps. These bumps are spaced on a 498µm array and range from 130-140µm in diameter and 25-27µm in height. This particular detector was designed at Caltech for the *High-Energy Focusing Telescope (HEFT)*, scheduled for a balloon-launched experiment sometime in 2004 [2]. The detector is attached to a custom low-noise analog VLSI readout chip that functions as a sensitive preamplifier for hard x-ray imaging. The VLSI chip has an identical array of Au-stud bumps that are aligned and mated to the epoxy bumps on the CZT detector. Due to the requirement for minimum noise, it was decided that no underfill epoxy would be used for this assembly. Mechanical integrity is therefore dependent upon the large number of epoxy bonds and approximate match in CTE of the materials being joined for the device to operate reliably at near-zero temperatures.

It was also required on this assembly that none of the bump epoxy come into contact with the pads on the VLSI chip. The ability to deposit a very precise mass and uniform shape of epoxy on the CZT pads, using the stencil printing technique, enabled the process to be adjusted for contacting only half of the single stud-bump's height of 44µm, as shown in Figure 5.

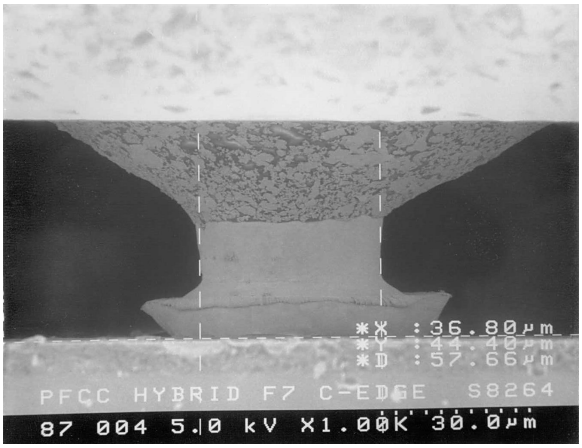

Figure 5: SEM image of a Au-stud bump centered within and connecting to a silver filled, conductive epoxy bump. Note that the epoxy does not reach the surface of the VLSI chip.

8. Hybrid (3D) Sensor Array Assembly

IR *focal-plane-arrays (FPR's)* connected to CMOS readout chips are the heart of advanced infrared imaging systems. Hybrid arrays, based on Z-plane technology, consist of multiple readout chips stacked and glued together into a cubic module that becomes a back plane multiplexer [3]. Electrical contacts of each silicon slice are routed onto their

respective edges and form a planar-array bed of contacts for the glued module. The IR sensor is then connected to the 3D module, forming a hybrid array.

Figure 6 illustrates a hybrid array that was developed as a test bed for evaluating various steps of the assembly process. It consists of a thin silicon test chip with 8000 connections organized in an 80 X 100 array of 'dog bone' shaped contacts (see Fig's. 7&8).

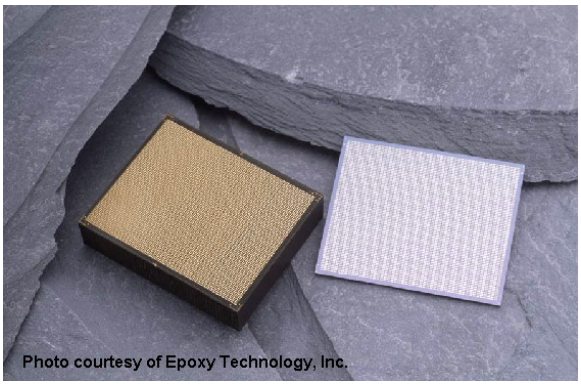

Figure 6: 8000 I/O sensor array test chip (right) and 3D-silicon back plane multiplexer module (left) prior to assembly (~17mm X 21mm).

When assembled to the 3D multiplexer module, a daisy-chained interconnection results, which allows segments within each double-row of contacts to be tested for opens and shorts between adjacent rows. Although a preliminary test piece, consisting of two silicon chips with the same pad structures, was successfully assembled and tested, the results from assembling the actual 3D hybrid array were inconclusive. Only one device was assembled and tested and that device had regions near the corners and edges of the hybrid that exhibited open connections after curing the epoxy at 80°C.

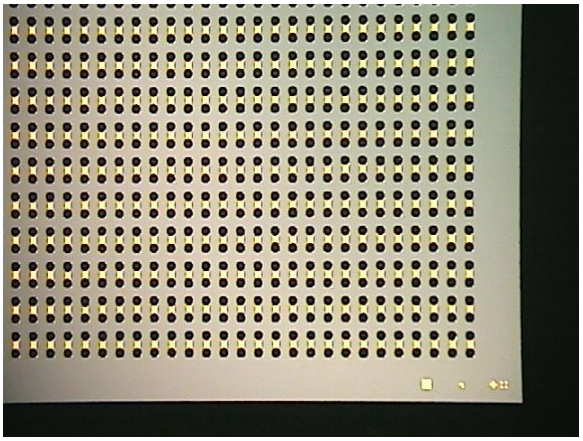

Figure 7: Portion of a sensor array test chip with 8000 connections in an 80 X 100 matrix with 200µm pitch.

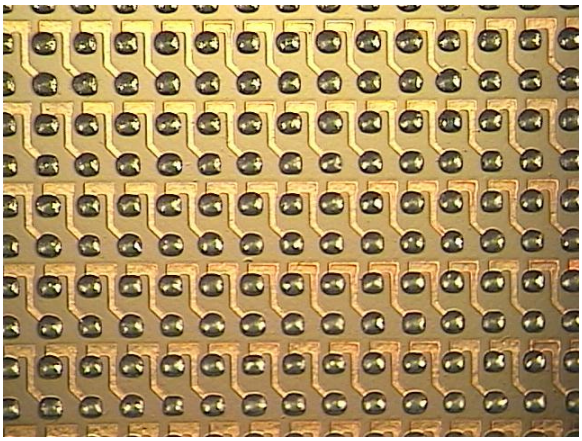

Figure 8: Close-up detail of conductive epoxy bumps on the 3D-silicon mutiplexer module of figure 5 (200µm pitch).

A mismatch in CTE properties between the thin silicon test chip and 3D module, that contained 49 separate glue lines (each 15µm thick) between 50 chip layers, was suspected as a possible cause.

9. Multi-stacked Au-stud bumps

Ensuring a uniform height for every bump within a large array of Au-stud bumps is largely a matter of controlling the diameter of the ball bumps and amount of wire ("*pig-tail*" length) that protrudes from the top of the ball bump. Simply pulling the wire until it breaks does not ensure a repeatable process (see Figure 9). A better method employs a shearing tool and/or coining technique immediately after the ball bump is thermosonically welded to the pad to establish a more consistent ball bump height [4].

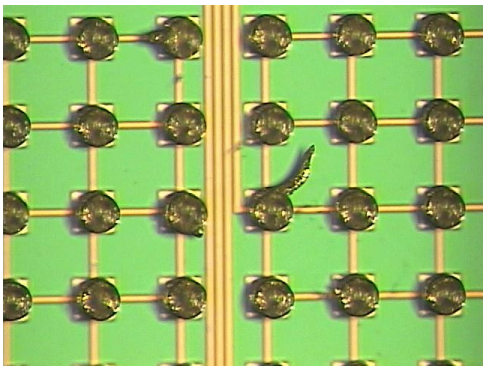

Figure 9: Photo of Au-stud bumps with protruding wires.

One of the more interesting and recent developments in Au-stud bump bonding has been the ability to stack multiple bumps atop one another to increase the 'stand-off' height. Figures 10 and 11 illustrate examples of double and triple ball bumps bonded directly on top of each other. The triple stud bump measures in excess of 100µm in height with

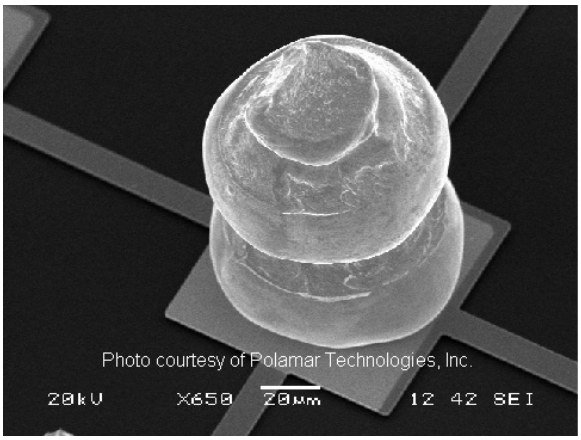

Figure 10: SEM Photo of a double-ball Au-stud bump.

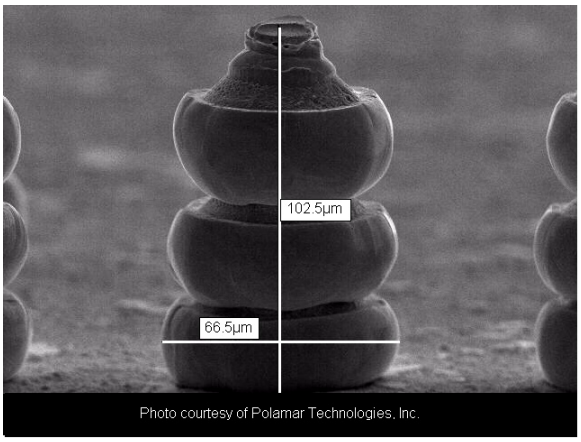

Figure 11: SEM Photo of a triple-ball Au-stud bump.

bump-to-bump uniformity reportedly held to within 5-7µm, well within the process window for working with stencil printed conductive adhesives. This extra height aids in decoupling some of the residual strain resulting from CTE mismatch and simplifies the under-filling process for large-area devices. It also provides a better low-noise interface for some applications.

Energy resolution of hard x-ray sensors, for example, may be adversely affected by the input capacitance between the anodes of a CdZnTe detector and plane of a VLSI preamplifier chip if the parts are mounted too closely together. This problem is compounded with separation distances between planes that are on the order of 8-15 microns using typical hybridization techniques.

Small variation in camber between the mounted surfaces can also cause the indium bumps to separate after removal of the normal forces applied during the fusion process. Consequently, there is an effort presently underway to try to increase indium bump-heights, without compromising the ability to deposit finer-pitched bumps. If the CdZnTe detector or IR focal plane array has a pixel spacing greater than 100µm, then consideration should be given to using a combination of Au-stud bumps with conductive epoxy to achieve a greater stand-off height between surfaces.

10. Future Trends

The minimum bump-pitch (and hence resolution) that can be achieved, using a stencil printed process, is presently limited by the distribution in size of silver flakes used to manufacture the conductive inks. The silver flakes typically range from 8-30µm in diameter and are rather flat and irregular in shape. Unless adequately coated with a lubricating film and held in suspension, the flakes can agglomerate into larger clumps that will clog the stencil apertures. This problem becomes more acute when trying to dispense or jet very small amounts of ink through a needle or orifice. The minimum dot size that can be uniformly deposited using a dispensing process is around 125 microns, whereas uniform bumps as small as 60-70 microns can be stencil printed.

Smaller silver flake is available, but is expensive due to the need for repetitive filtering techniques to isolate the smaller flakes from the larger matrix. With continuing improvement in manufacturing methods of nano-sized conductive materials, the cost may decrease to the point that they become a practical substitute for silver flake used in present formulations. These newer materials should enable even finer printing resolutions and make it practical to develop desktop bumping equipment based on ink-jet technology. Progress toward this possibly has already been demonstrated in university labs [5]. Until then, the stencil printing process remains the best technique for achieving high-resolution, uniform dots or bumps using traditional conductive epoxies.

11. Conclusion

In summary, as Au-stud bump diameters decrease and conductive materials and application techniques improve, it may be entirely feasible for this technology to be substituted for flip chip applications that are presently dependant upon indium bump bonding or electroplated solder for very fine pitch, high pin count applications. The techniques described in this article may also be adapted for future optical chip-to-chip interconnect using fiber-optic columns bonded with stencil printed (optically translucent) epoxy bumps.

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