Adhesive Interconnect Flip Chip Assembly

BY JAMES E. CLAYTON

The search for lead solder alternatives is stimulating interest in isotropic conductive adhesive assembly for flip chip interconnection. Originally found principally in low bump count and low cost applications such as smart cards, adhesive assembly has now moved upscale to applications such as implanted medical devices and large imaging (IR and x-ray/gamma-ray) detector arrays. While indisputably lead-free, the many other advantages of adhesive over solder bump flip chip assembly clearly foretell a wider role for adhesive flip chip assembly in tomorrow's demanding products.

Lead is not the only thing that vanishes with adhesive assembly. Since adhesives require no fluxing, the post cleaning required to remove flux residues also vanishes. The problems that flux residues cause in underfill delamination and in long-term reliability similarly vanish with the fluxes.

Adhesive assemblies emerge from the curing oven ready for underfill, if required. The more compliant gold bumps and adhesive can tolerate higher thermal expansion differences between chip and substrate without underfill. Large arrayed silicon detectors with thousands of connections often do not require any underfill, since they are assembled to thermally matched silicon readout chips.

Adhesives are suitable for extremely high density interconnects, presently dominated by indium bump bonding, also known as "hybridization." Hybridization requires indium bumps on both mating surfaces, cold-welded by applying high pressure. Adhesive assembly arrays with bump pitches as low as 50 µm are much less costly than indium hybridization.

Common adhesive cure temperatures of 150°C and below are far lower than today's eutectic solder, and far lower than candidate lead-free solders. For temperature sensitive materials, such as compound semiconductors, or polymer-based devices such as pyro-electric detectors, adhesive cure temperatures may be less than 80°C. Special low curing temperature adhesive formulations allow room temperature curing when needed.

Gold stud bumps commonly are combined with adhesive attachment. Although direct gold-to-gold interconnection, with no adhesive, is a reliable flip chip technique, the required high thermocompression forces limit it to lower bump counts. In contrast, gold stud bumps placed into conductive adhesive bumps require very low normal forces, making this method suitable for large chips with thousands of connections.

Stud bumps can be placed directly on an IC's standard aluminum bond pads with no special preparation, although a light plasma cleaning may be used to remove any contamination on the pads. The costly and complicated multi-step process of under bump metallization required for solder bumping is eliminated. Whole wafers, partial wafers, or even individual diced chips can be easily gold stud bumped, eliminating the dependency on processing full-wafers which is typical of most solder bumping processes.

Adhesive attachment may relax the process window for coplanarity. The adhesive itself compensates for small variations in stud bump height. The adhesive also can be used to identify bumps that may be excessively low, by visually inspecting for adequate epoxy transfer onto all bumps before curing the adhesive.

If high pin count die make sequential stud bumping of an entire wafer unacceptably slow, electroplated gold bumps offer an alternative. The main advantages of electroplated bumps are the bumping time per wafer, and a higher overall bump height if thick photoresist is used.

The isotropic conductive adhesives (ICA) commonly combined with gold stud bumps are epoxies loaded with up to 80% silver flakes, ranging from 5 to 30 µm in diameter. The flakes tend to lie atop one another like a pile of wet leaves. Cured ICA has the same electrical conductivity in all directions (isotropic). More expensive gold, palladium or platinum flakes are used in those applications, such as implanted medical devices, which are not compatible with silver.

Carbon nanotubes currently are being tested as a potential alternative to silver flakes. At present, they are quite expensive. In addition, nanotubes have a strong tendency to agglomerate, preventing a uniform distribution of the conductors when mixed into a resin matrix.

In summary, the emerging trend towards a gold-bump/adhesive system brings with it a demonstrated, well-tested solution for low-temperature, flux-free, lead-free, flip chip assembly. However, beyond those obvious advantages, the low temperature assembly and manufacturing flexibility of gold bump adhesive assembly link it closely to the latest trends in semiconductor and sensor device development. Looking toward a future world of "plastic" ICs, polymer memory chips, and a variety of sensors fashioned from compound semiconductors, gold bump conductive adhesive may become the only practical, economical choice for low temperature flip chip assembly. **AP**

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